FIG.1

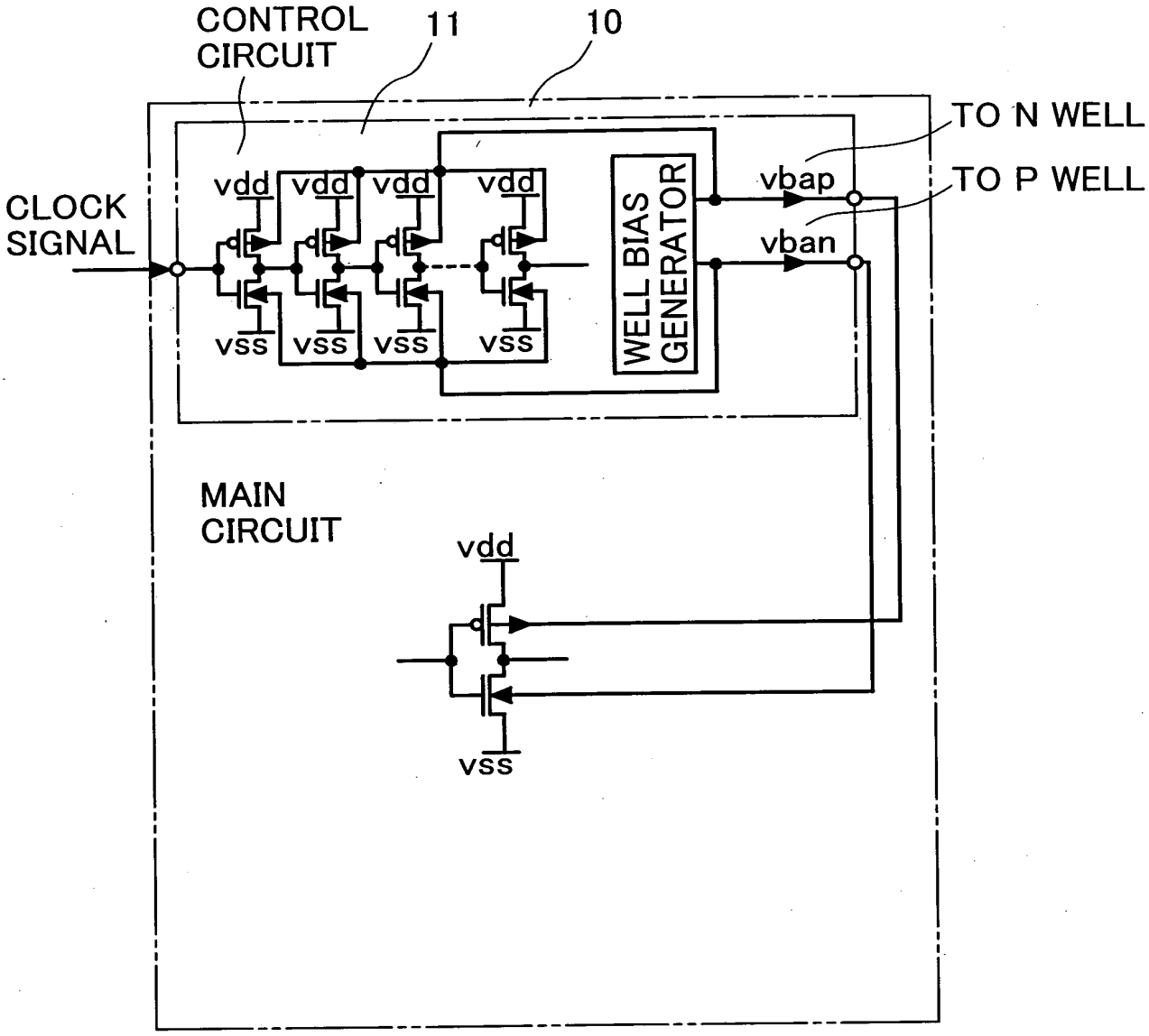

CONTROL CIRCUIT
11
10
TO N WELL
TO P WELL
CLOCK SIGNAL
vdd
vdd
vdd
vdd
vss
vss
vss
vss
WELL BIAS GENERATOR
vbap
vban
MAIN CIRCUIT
vdd
vss

FIG.2

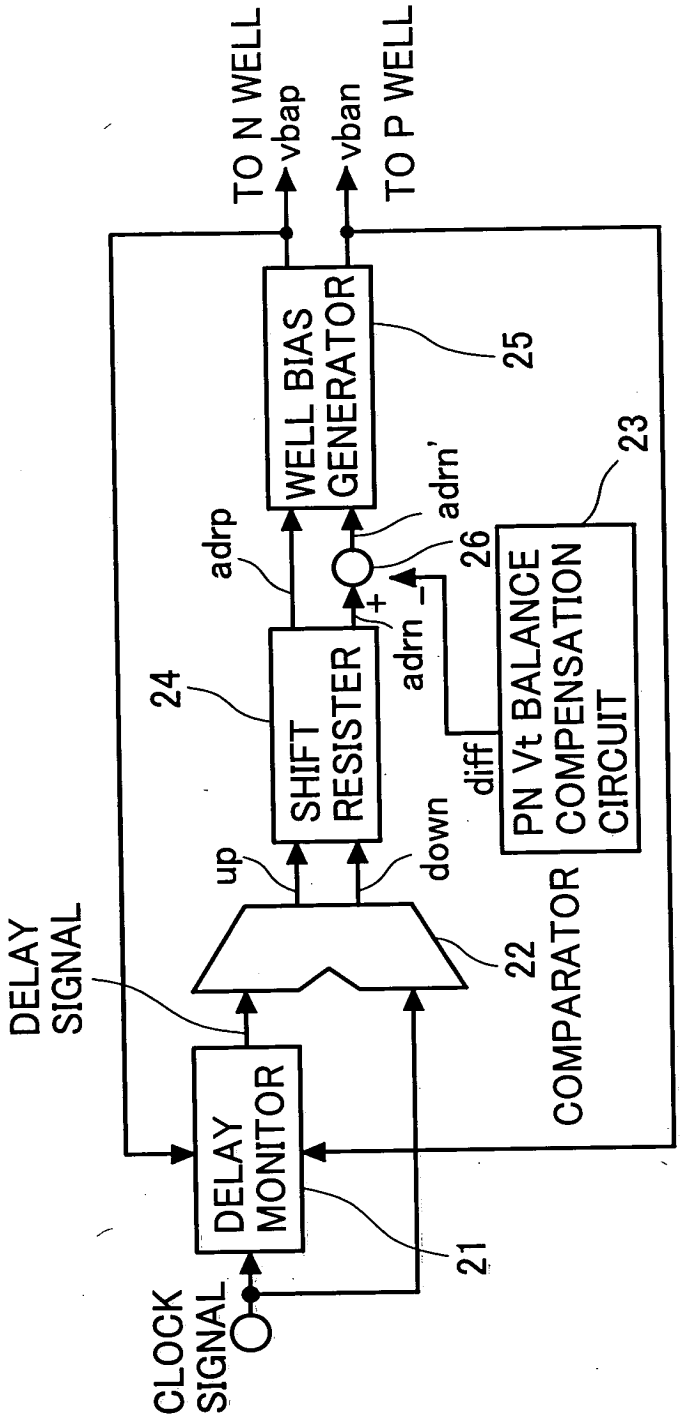

TO N WELL
vbap
vban
TO P WELL
WELL BIAS GENERATOR
25
adrp
adrn'
26
23
PN Vt BALANCE COMPENSATION CIRCUIT
24
SHIFT RESISTER
adrn
diff
up
down
DELAY SIGNAL
22
COMPARATOR
DELAY MONITOR
21
CLOCK SIGNAL

FIG.3

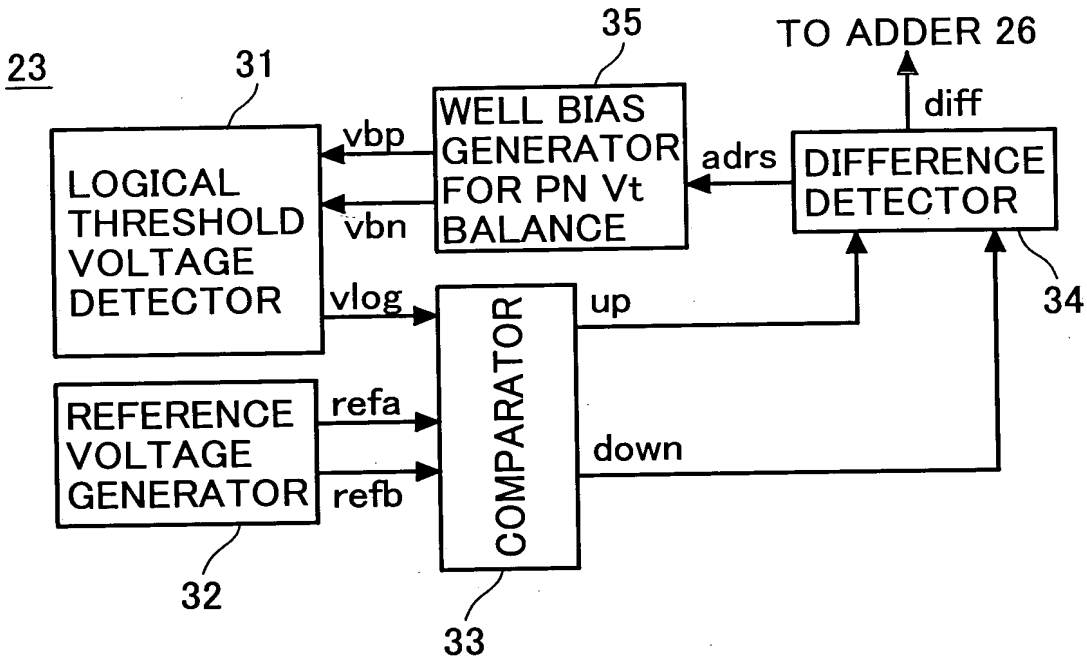

23
31
35
TO ADDER 26
diff
WELL BIAS GENERATOR FOR PN Vt BALANCE
vbp
vbn
adrs
DIFFERENCE DETECTOR
LOGICAL THRESHOLD VOLTAGE DETECTOR
vlog
COMPARATOR
up
down
34
REFERENCE VOLTAGE GENERATOR
refa
refb
32
33

FIG.4

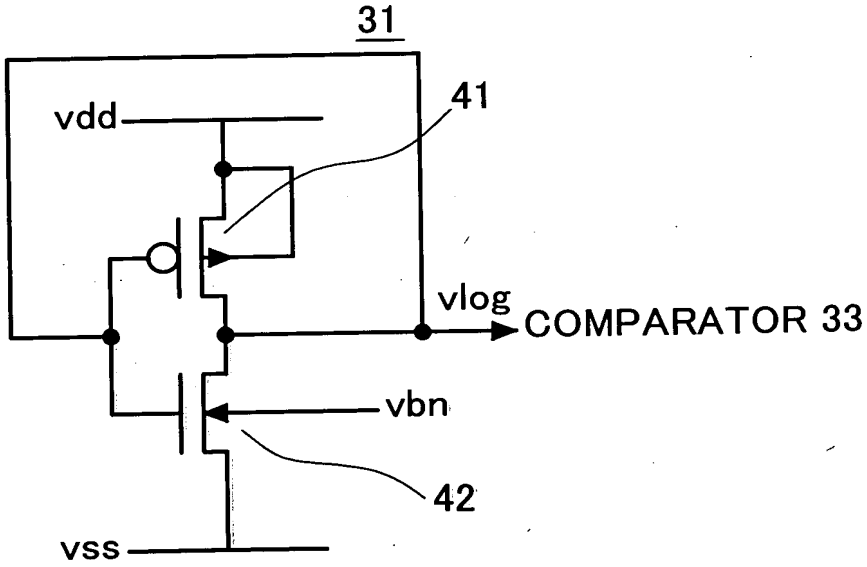

31
vdd
41
vlog
COMPARATOR 33
vbn
42
vss

FIG.5

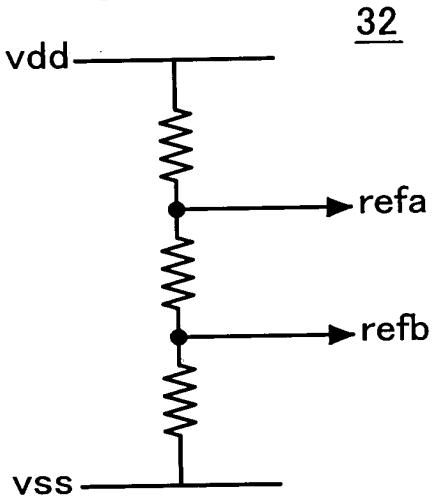

32
vdd
refa
refb
vss

FIG.6

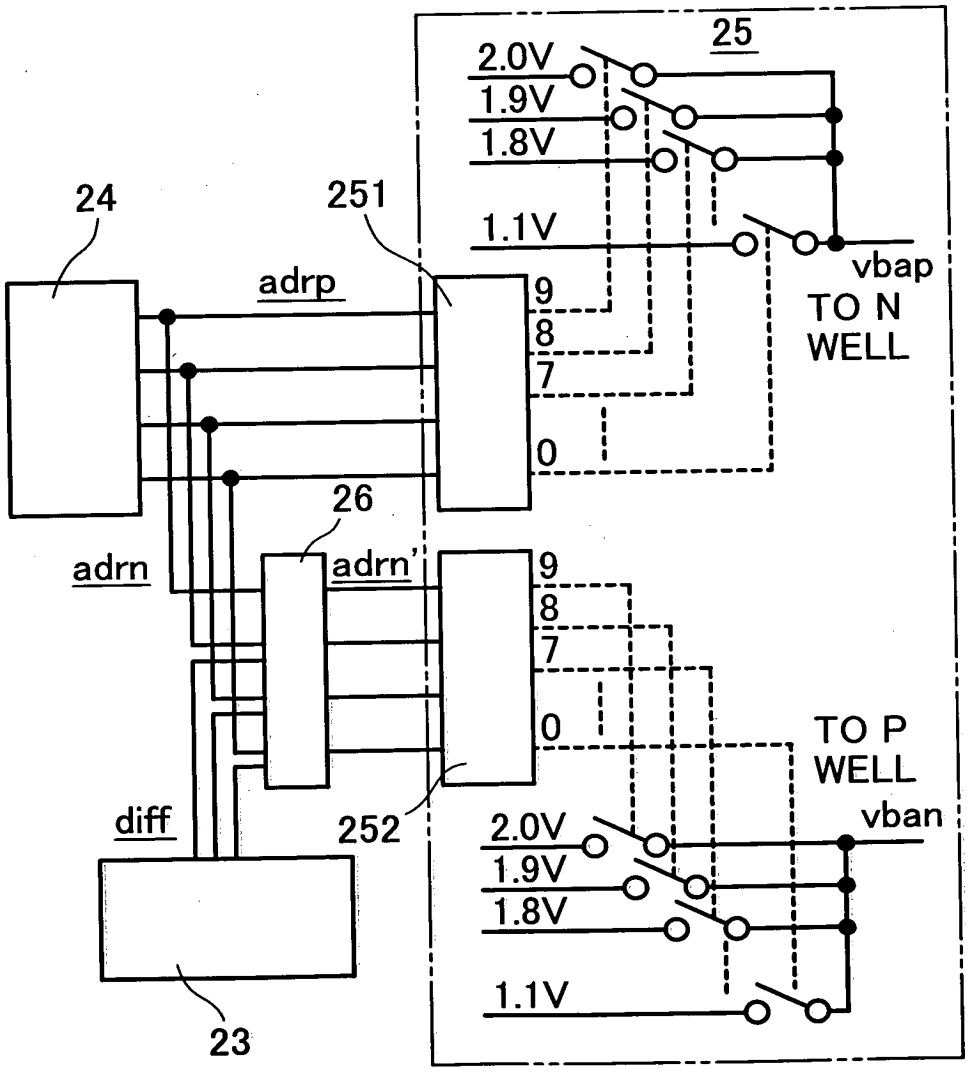

25
2.0V
1.9V
1.8V
1.1V
vbap
TO N WELL
24
251
adrp
9
8
7
0
26
adrn
adrn'
9
8
7
0
TO P WELL
vban
diff
252
2.0V
1.9V
1.8V
1.1V
23

FIG.7

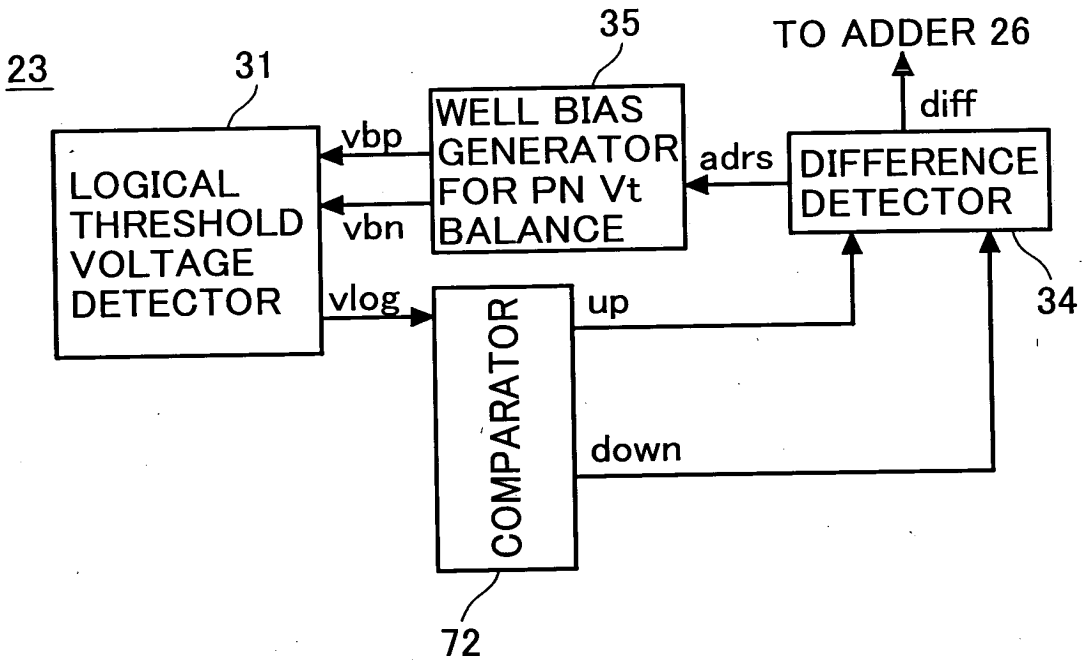

23
31
35
TO ADDER 26
diff
LOGICAL THRESHOLD VOLTAGE DETECTOR
vbp
vbn
WELL BIAS GENERATOR FOR PN Vt BALANCE
adrs
DIFFERENCE DETECTOR
34
vlog
COMPARATOR
up
down
72

FIG.8

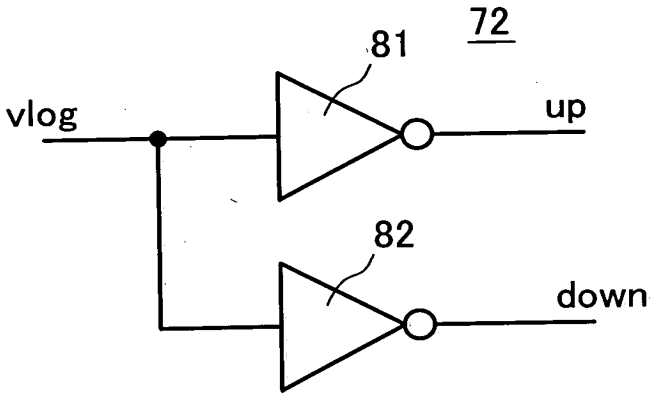

72
81
vlog
up
82
down

FIG.9

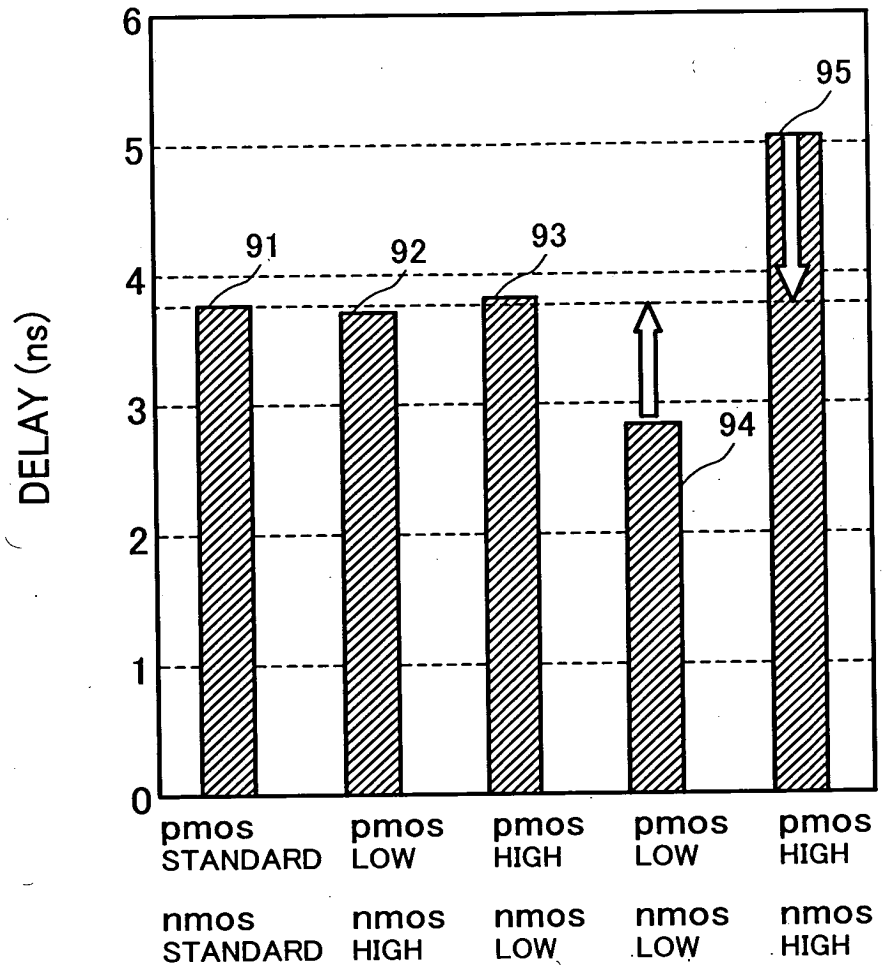

6
5
4
3
2
1
0
DELAY (ns)
91
92
93
94
95
pmos STANDARD
pmos LOW
pmos HIGH
pmos LOW
pmos HIGH
nmos STANDARD
nmos HIGH
nmos LOW
nmos LOW
nmos HIGH
DEVICE THRESHOLD VOLTAGE VARIATION

FIG.10

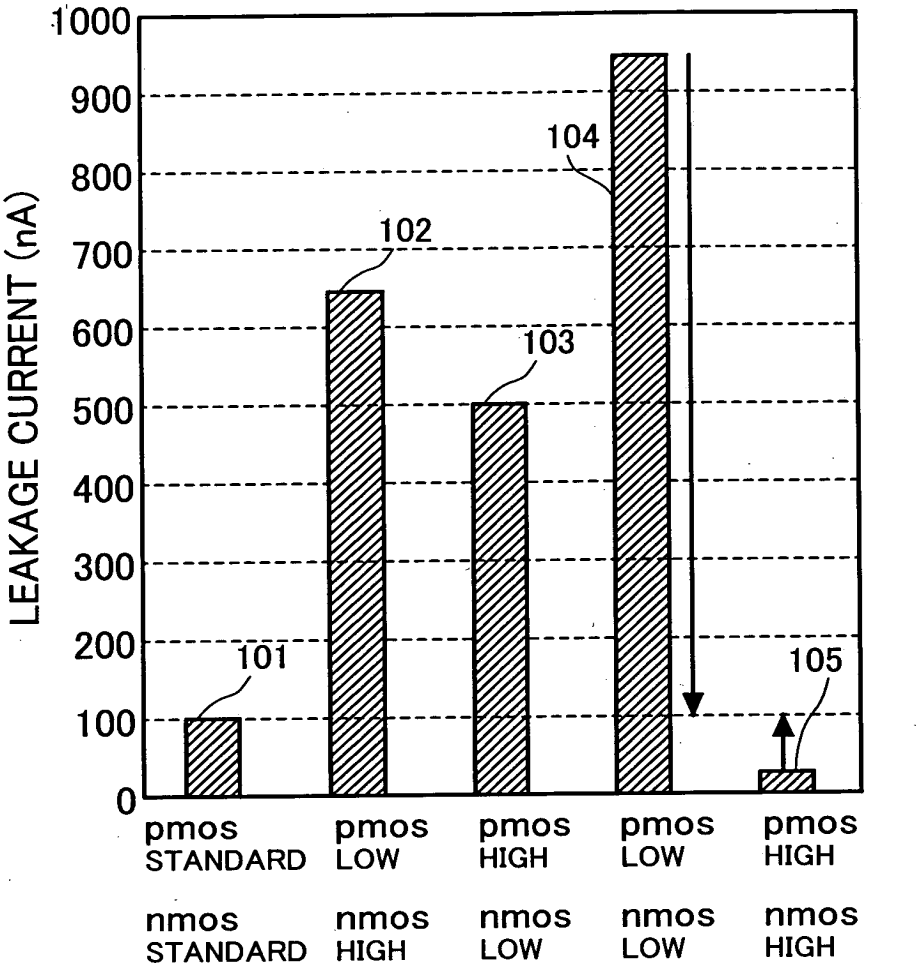

LEAKAGE CURRENT (nA)
1000
900
800
700
600
500
400
300
200
100
0
101
102
103
104
105
pmos STANDARD
pmos LOW
pmos HIGH
pmos LOW
pmos HIGH
nmos STANDARD
nmos HIGH
nmos LOW
nmos LOW
nmos HIGH
DEVICE THRESHOLD VOLTAGE VARIATION

FIG.11

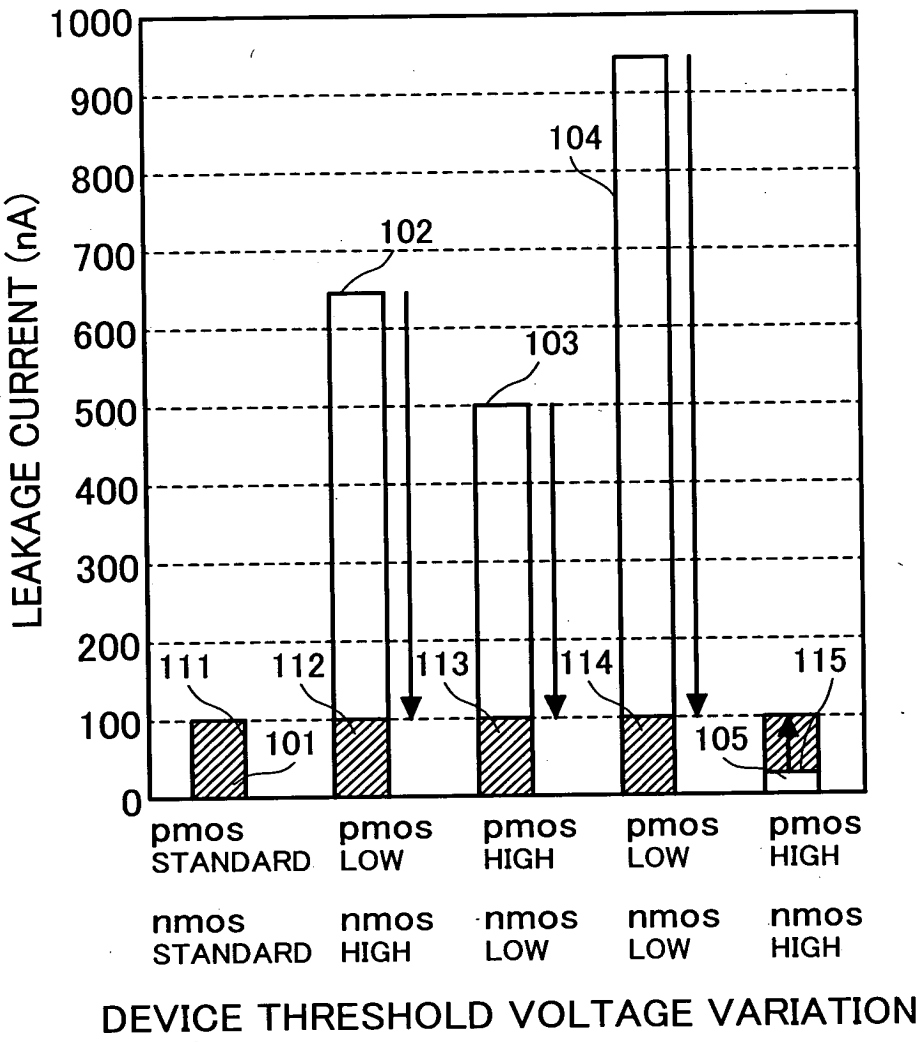

1000
900
800
700
600
500
400
300
200
100
0
LEAKAGE CURRENT (nA)
104
102
103
111
112
113
114
115
101
105
pmos STANDARD
pmos LOW
pmos HIGH
pmos LOW
pmos HIGH
nmos STANDARD
nmos HIGH
nmos LOW
nmos LOW
nmos HIGH
DEVICE THRESHOLD VOLTAGE VARIATION

FIG.12

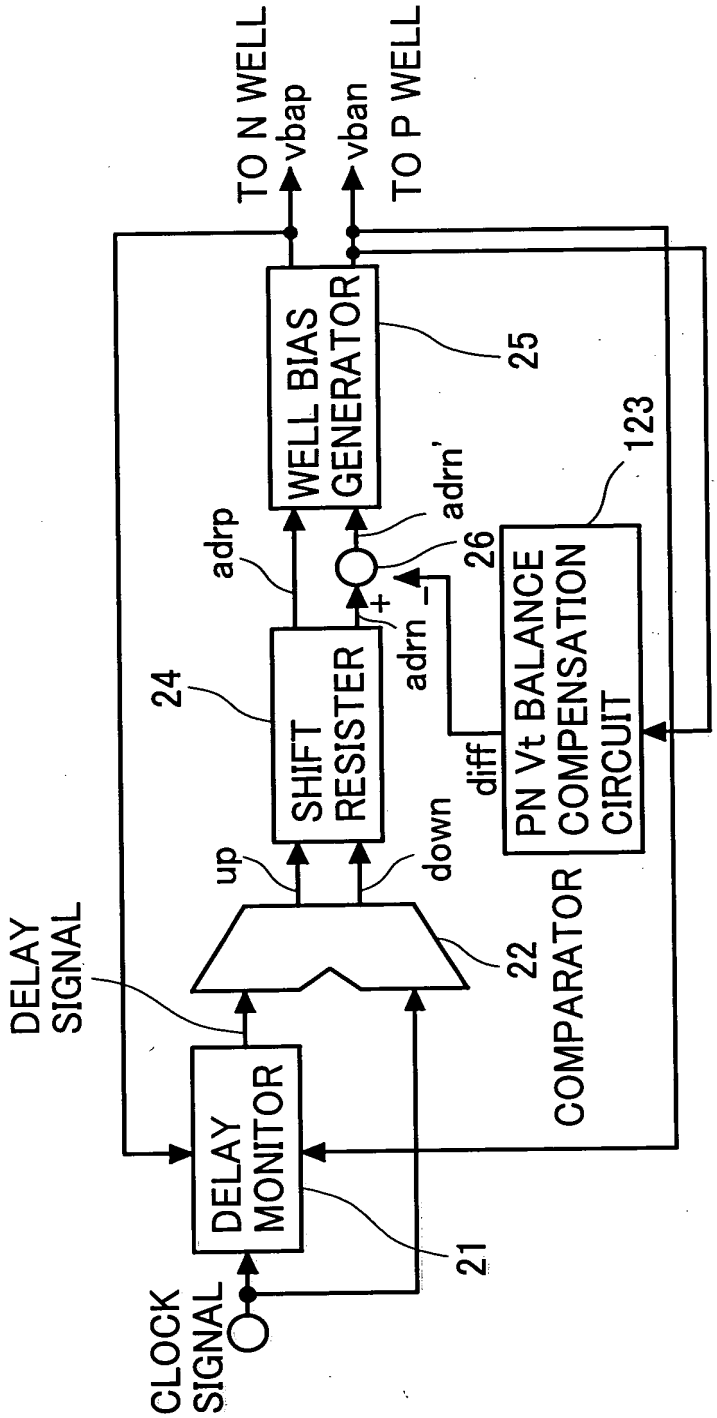

TO N WELL
vbap
vban
TO P WELL
WELL BIAS GENERATOR
25
123
adrn'
adrp
26
+
adrn –
24
SHIFT RESISTER
diff
PN Vt BALANCE COMPENSATION CIRCUIT
up
down
DELAY SIGNAL
22
COMPARATOR
DELAY MONITOR
21
CLOCK SIGNAL

FIG.13

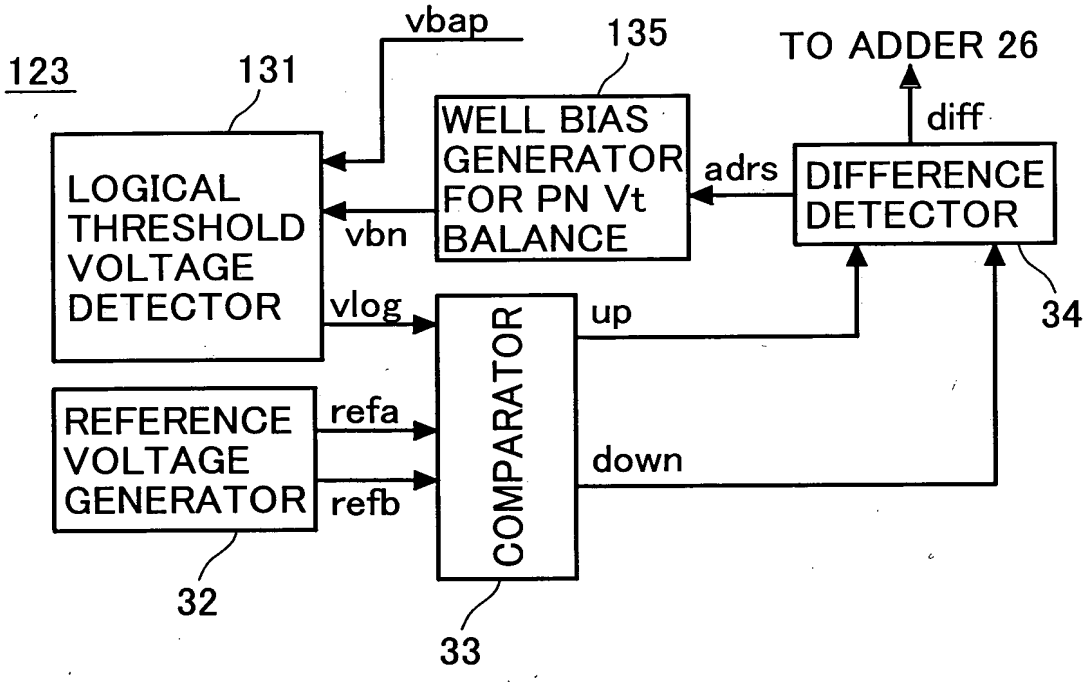

123
131
vbap
135
TO ADDER 26
diff
WELL BIAS GENERATOR FOR PN Vt BALANCE
adrs
DIFFERENCE DETECTOR
LOGICAL THRESHOLD VOLTAGE DETECTOR
vbn
vlog
COMPARATOR
up
down
34
REFERENCE VOLTAGE GENERATOR
refa
refb
32
33

FIG.14

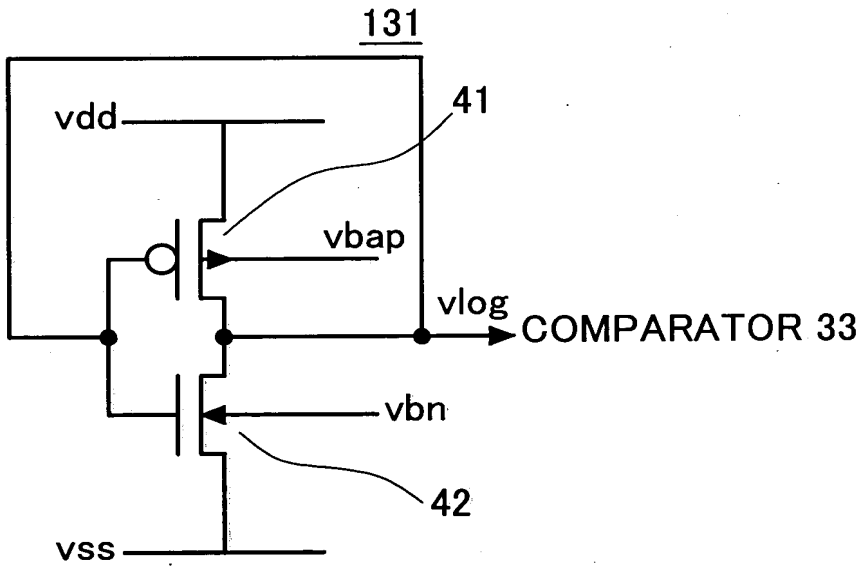

131
vdd
41
vbap
vlog
COMPARATOR 33
vbn
42
vss

FIG.15

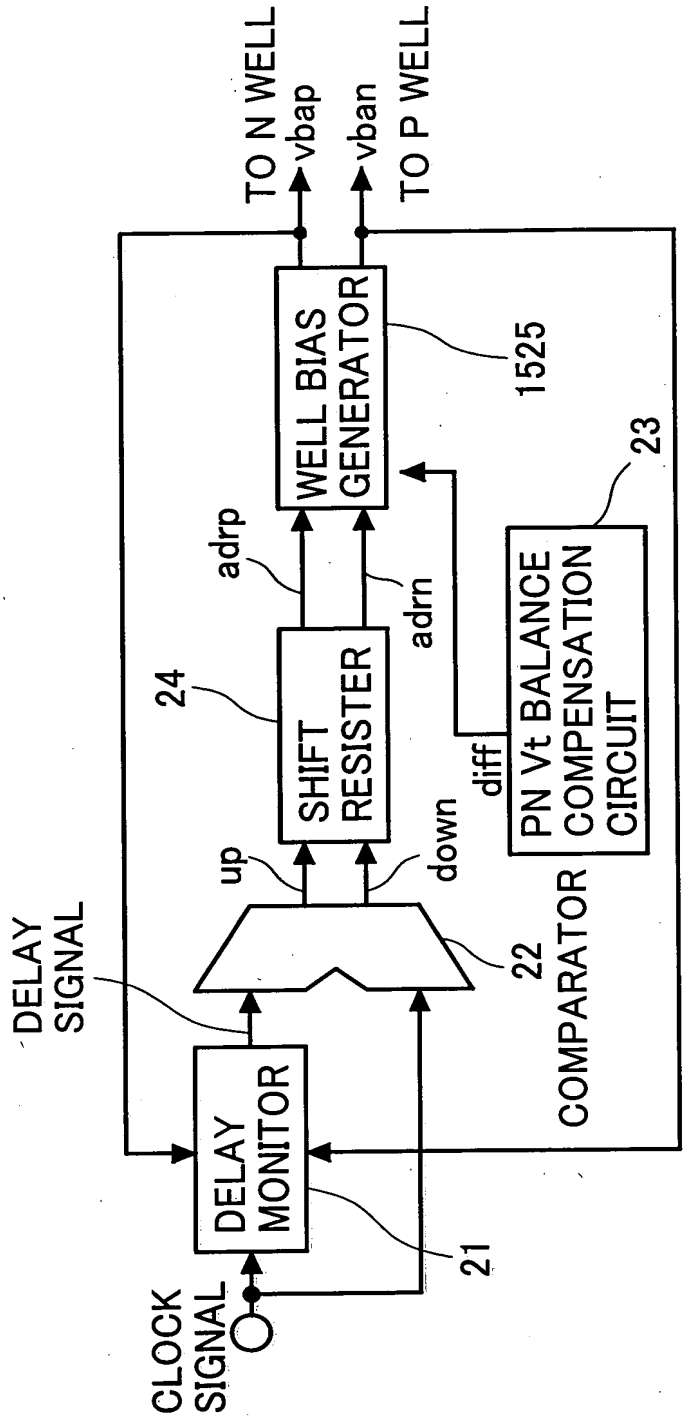

TO N WELL
vbap
vban
TO P WELL
WELL BIAS GENERATOR
1525
23
adrp
adrn
24
SHIFT RESISTER
diff
PN Vt BALANCE COMPENSATION CIRCUIT
up
down
DELAY SIGNAL
22
COMPARATOR
DELAY MONITOR
21
CLOCK SIGNAL

FIG.16

diff	adrp	adrn
−3	9	9
	8	9
	7	9
	6	8
	5	7
	4	6
	3	5
	2	4
	1	3
	0	2
−2	9	9
	8	9
	7	8
	6	7
	5	6
	4	5
	3	4
	2	3
	1	2
	0	1
−1	9	9
	8	8
	7	7
	6	6
	5	5
	4	4
	3	3
	2	2
	1	1
	0	0

diff	adrp	adrn
0	9	8
	8	7
	7	6
	6	5
	5	4
	4	3
	3	2
	2	1
	1	0
	0	0
1	9	7
	8	6
	7	5
	6	4
	5	3
	4	2
	3	1
	2	0
	1	0
	0	0
2	9	6
	8	5
	7	4
	6	3
	5	2
	4	1
	3	0
	2	0
	1	0
	0	0

FIG.17

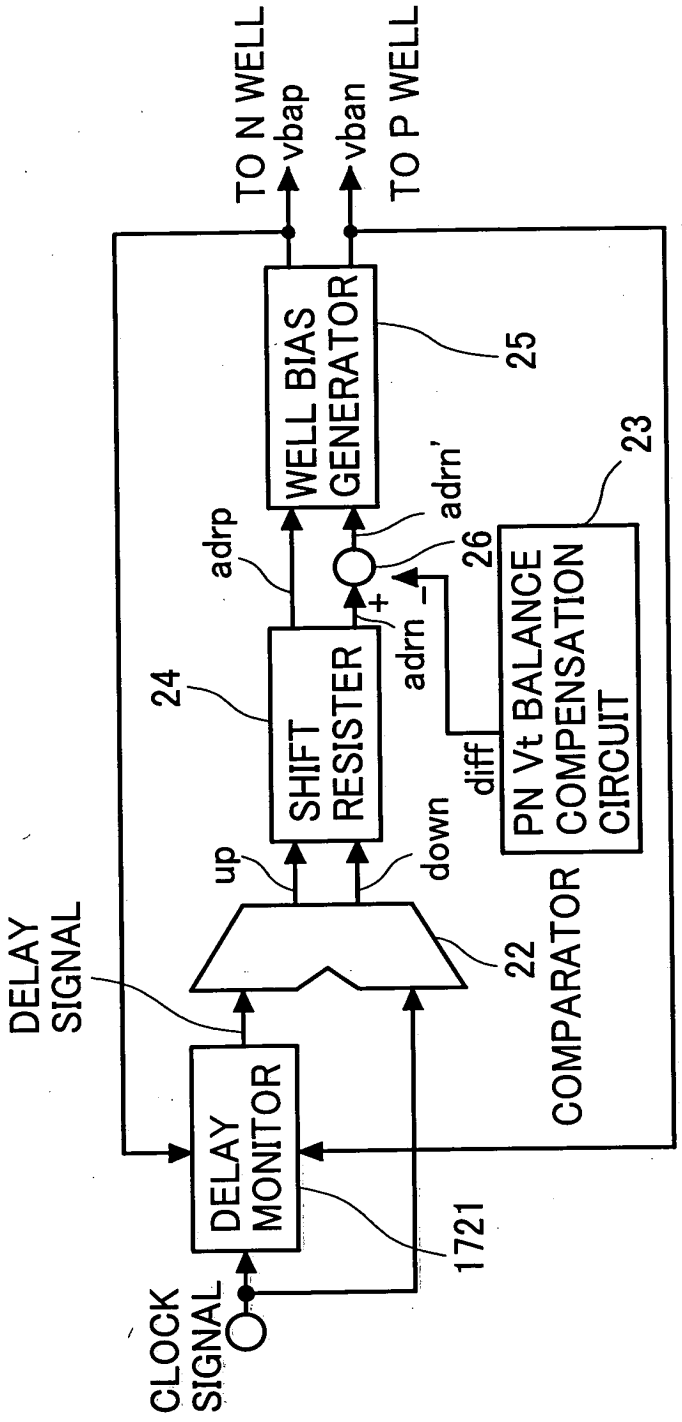

TO N WELL
vbap
vban
TO P WELL
WELL BIAS GENERATOR
25
adrp
adrn'
26
23
24
SHIFT RESISTER
adrn
+
−
diff
PN Vt BALANCE COMPENSATION CIRCUIT
up
down
DELAY SIGNAL
22
COMPARATOR
DELAY MONITOR
1721
CLOCK SIGNAL

FIG.18

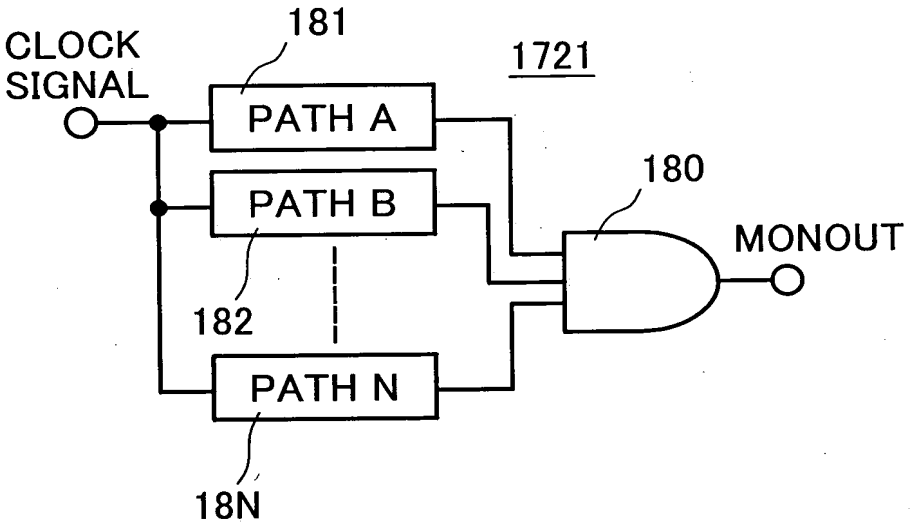


FIG.19A

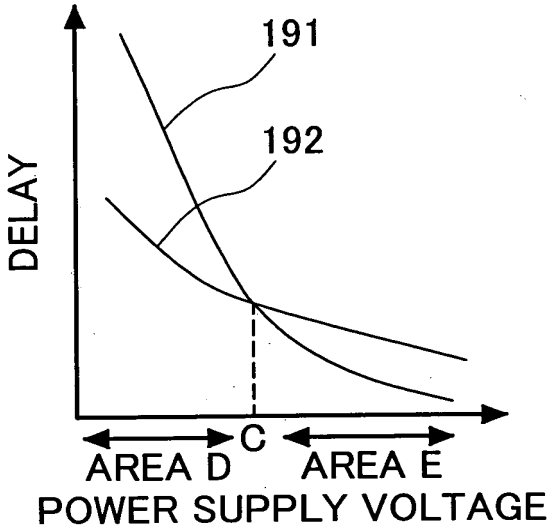


FIG.19B

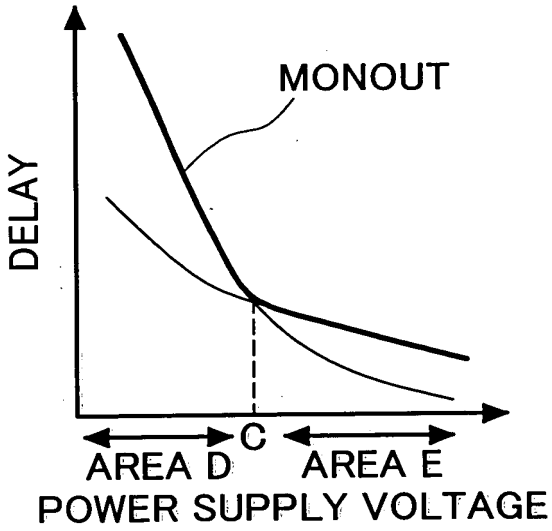
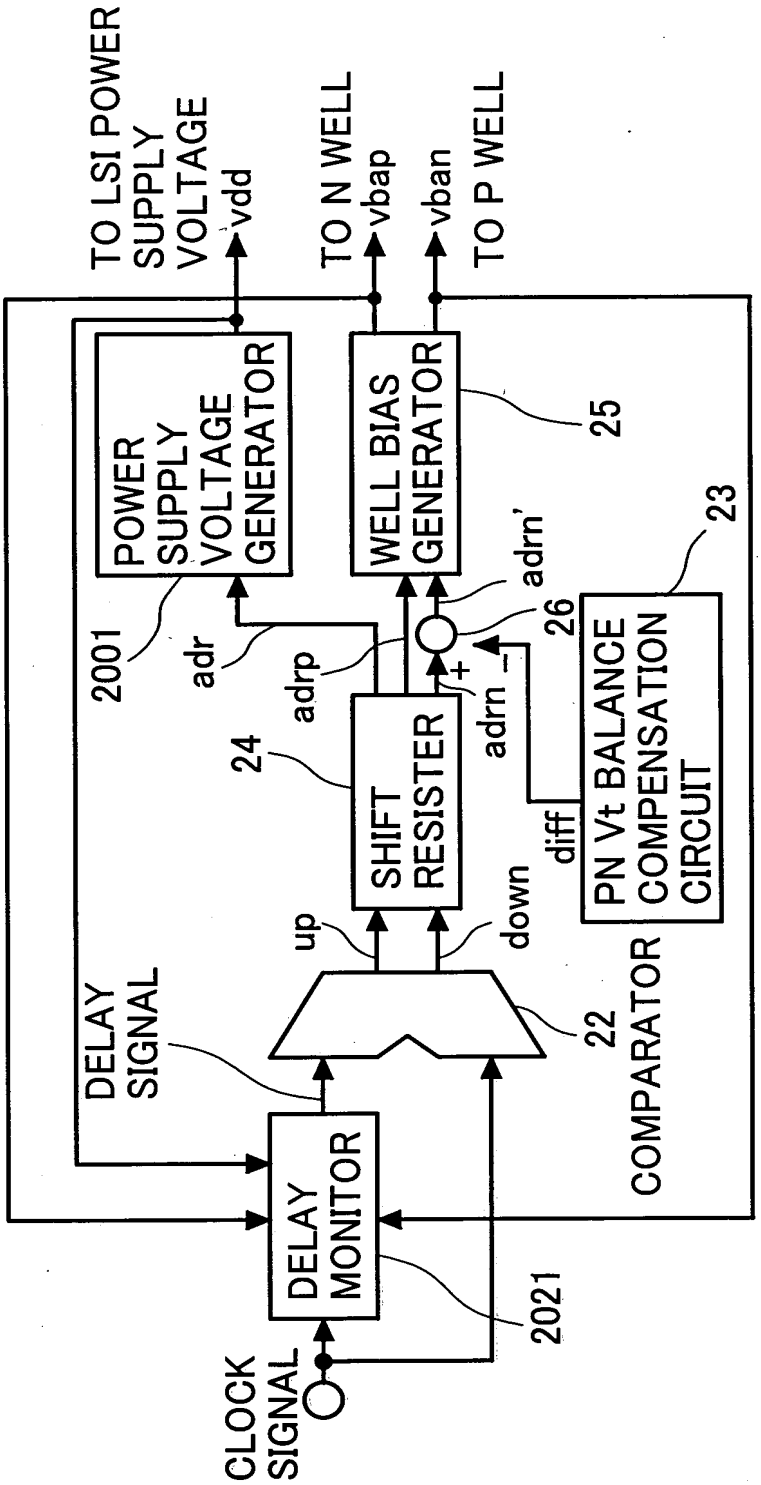


FIG.20


TO LSI POWER SUPPLY VOLTAGE
vdd
TO N WELL
vbap
vban
TO P WELL
POWER SUPPLY VOLTAGE GENERATOR
2001
WELL BIAS GENERATOR
25
adr
adrp
adrn'
26
23
24
SHIFT RESISTER
adrn
diff
PN Vt BALANCE COMPENSATION CIRCUIT
up
down
DELAY SIGNAL
22
COMPARATOR
DELAY MONITOR
2021
CLOCK SIGNAL